

**WHAT IS CLAIMED IS:**

1        1.        An integrated memory system, comprising at least a non-volatile memory and  
2        an automatic storage error corrector, characterized in that the memory system  
3        comprises circuit means, functionally independent, each of them being responsible  
4        for the correction of a predetermined storage error; at least one of said means  
5        generating a signal to ask a correction being external to the memory.

1        2.        A system according to claim 1, characterized in that said memory is  
2        connected to a controller by means of an interface bus and said means are  
3        incorporated both in the memory and in the controller.

1        3.        A system according to claim 1, characterized in that in the memory said  
2        means comprise:

3                circuits for the coding required to correct two errors;

4                a logic for calculating the syndrome;

5                a circuit for correcting a single error;

6                a logic for detecting more than one error.

1        4.        A system according to claim 3, characterized in that said means also  
2        comprise:

3                a logic for bringing to the controller:

4                        a one-or-no-error-corrected data ;

5                        the uncorrected error; and

6                        the calculated syndrome .

1        5.        A system according to claim 2, characterized in that said means comprise a  
2        circuit for generating a signal activated to request the external correction of an error  
3        by said controller.

1        6.        A system according to claim 3, characterized in that said coding block is  
2        located immediately downstream of the input terminal of said memory and performs  
3        a vector product proportional to the number of parity bits and obtained through the  
4        synthesis of a corresponding logic function.

1 7. A system according to claim 6, characterized in that said logic for calculating  
2 the syndrome uses again the parity calculation circuit of the coding block.

1 8. A system according to claim 3, characterized in that said circuit for correcting  
2 a single error comprises a block for decoding a single error effective to recognise  
3 each of the several syndromes associated to a single error to activate, through a  
4 corresponding vector, the correction of the corresponding bit.

1 9. A system, comprising:

2 a first circuit operable to store data having associated therewith at least one  
3 storage error of a plurality of storage-error types, the first circuit operable to correct a  
4 first-type error of the plurality of storage-error types; and

5 a second circuit coupled to the first circuit, the second circuit operable to  
6 correct a second-type error of the plurality of storage-error types.

1 10. The system of claim 9 wherein the second circuit is operable to generate a  
2 signal requesting correction of a third-type error of the plurality of storage-error  
3 types.

1 11. The system of claim 9 wherein the first circuit is further operable to determine  
2 at least one syndrome associated with the at least one storage error.

1 12. The system of claim 9 wherein the first circuit is further operable to detect the  
2 second-type error.

1 13. The system of claim 9 wherein the second circuit corrects the second-type  
2 error in response to a signal generated by the first circuit.

1 14. The system of claim 9 wherein the first circuit comprises a non-volatile  
2 memory.

1 15. The system of claim 9 wherein:

2 the first circuit is disposed on a first integrated circuit; and

3 the second circuit is disposed on a second integrated circuit.

1 16. The system of claim 9 wherein the first and second circuits are disposed on  
2 an integrated circuit.

1 17. A memory device, comprising:

2 a storage portion operable to store data having associated therewith at least  
3 one storage error of a plurality of storage-error types;

4 a first circuit operable to correct a first-type error of the plurality of storage-  
5 error types; and

6 a second circuit operable to generate a signal indicating detection of a  
7 second-type error of the plurality of storage-error types.

1 18. The device of claim 17, further comprising a third circuit operable to determine  
2 at least one syndrome associated with the at least one storage error.

1 19. A method, comprising:

2 storing, in a memory location of a device, data having associated therewith at  
3 least one storage error of a plurality of storage-error types; and

4 correcting, at the memory location, a first-type error of the plurality of storage-  
5 error types.

1 20. The method of claim 19, further comprising generating, at the memory  
2 location, an interrupt-request signal indicating detection of a second-type error of the  
3 plurality of storage-error types.

1 21. An electronic system, comprising:

2 a first integrated circuit having a memory operable to store data having  
3 associated therewith at least one storage error of a plurality of storage-error types,  
4 the memory operable to correct a first-type error of the plurality of storage-error  
5 types; and

6 a second integrated circuit coupled to the first circuit, the second integrated  
7 circuit having processor operable to correct a second-type error of the plurality of  
8 storage-error types.